REMARKS

Claims remaining in the present patent application are numbered 1-20. The rejections and comments of the Examiner set forth in the Office Action dated November 10, 2004 have been carefully considered by the Applicants. Applicants respectfully request the Examiner to consider and allow the remaining claims.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include reference characters not in mentioned in the description. Applicants have herein amended the specification to include the objected to reference characters in compliance with 37 CR 1.121(b). No new matter has been added. As such, Applicants respectfully contend that the drawing objections are moot at this time.

§112 Rejection

The present Office Action rejected Claims 1-20 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. That is, the claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Namely it is not understood what MIN VT=1V,

VT1=3V, VT2=5V and VT3 =7V in Fig. 2A CONVENTIONAL ART; all elements in Fig. 2B CONVENTIONAL ART; VTMIN and VT in Fig. 3 CONVENTIOANL ART; VT MIN=1V in Fig. 5 CONVENTIONAL ART; VS=0V in Fig. 6; 806 and VT=VT MIN in Fig. 8A; VG=6V, VG=0V, VD=5V, VD=0V, VT=VT MIN, 846, 843 and 831 in Fig. 8B; VT=VT MIN in Fig. 8C really are. Applicants respectfully contend that one skilled in the art would be able to make and use the claimed invention using the application as guide.

Applicants respectfully contend that in Conventional Art Figure 2A, sufficient description is provided for the characters MIN VT=1V, VT1=3V, VT2=5V and VT3 =7V. As amended in the paragraph beginning on page 3, line 7, the MLC is programmed to various threshold levels VT. For example, to program the MLC at the threshold levels MIN VT, VT1, VT2, and VT3, the charge at that level must reach the assigned threshold voltages, as is well known in the art. For example, "bit combination '10' is represented by a first threshold voltage VT1 (e.g., VT1=3V), etc. As such, Applicants assert that the characters MIN VT=1V, VT1=3V, VT2=5V and VT3 =7V have overcome the 112 objection. Applicants respectfully request review and approval of Claims 1-20.

Applicants respectfully contend that in Conventional Art Figure 2B, sufficient description is provided for all elements in Fig. 2B CONVENTIONAL ART. As amended in the

paragraph beginning on page 3, line 15, the MLC is programmed to various threshold levels VT. For example, to program the MLC at the threshold levels MIN VT, VT1, VT2, VT3, VT4, VT5, VT6, and VT7 the charge at that level must reach the assigned threshold voltages, as is well known in the art. For example, "bit combination '111' is represented by a first threshold voltage VT=VT MIN (e.g., VT=VT MIN=1V), etc. As such, Applicants assert that the characters MIN VT, VT1, VT2, VT3, VT4, VT5, VT6, and VT7 of Figure 2B have overcome the 112 objection. Applicants respectfully request review and approval of Claims 1-20.

Applicants respectfully contend that in Conventional Art Figure 3, sufficient description is provided for VT MIN and VT in Fig. 3 CONVENTIONAL ART. As amended in the paragraph beginning on page 4, line 1, a graphical representation of the statistical deviation of multiple programmed threshold voltage levels is shown according to the conventional art. As shown in Figure 3, the threshold voltage VT at a minimum VT MIN is 1 volt (e.g., VT=VT MIN=1V) for programming the MLC at that level. As such, Applicants assert that the VT and VT MIN in Figure 3 Conventional Art have overcome the 112 objections. Applicants respectfully request review and approval of Claims 1-20.

Applicants respectfully contend that in Conventional Art Figure 5, sufficient description is provided for VT MIN=1V in

Fig. 5 CONVENTIONAL ART. As amended in the paragraph beginning on page 5, line 1, a timing diagram is shown where the threshold voltage 505 gradually rises from a minimum threshold voltage (e.g., $V_{T\ MIN}$=1V) to threshold voltage 505 (e.g., Vt2=5V). As such, Applicants assert that the VT MIN=1V in Figure 5 Conventional Art has overcome the 112 objections. Applicants respectfully request review and approval of Claims 1-20.

Applicants respectfully contend that in Figure 6, sufficient description is provided for VS=0V. As amended in the paragraph beginning on page 9, line 1, a source voltage (e.g., VS=0V) is also applied when programming the MLC. As such, Applicants assert that the VS=0V in Figure 6 has overcome the 112 objections. Applicants respectfully request review and approval of Claims 1-20.

Applicants respectfully contend that in Figure 8A, sufficient description is provided for 806 and VT=VT MIN. As amended in the paragraph beginning on page 10, line 13, the drain current 810 decreases as a result of the increasing threshold voltage 805 from V_T=$V_{T\ MIN}$ to V_T=3V effectively blocking the gate voltage 820 from inducing a conducting channel in the MLC, where the VT MIN =1V. In addition, Figure 8A clearly shows and the description describes that the threshold voltage 805 reaches the desired level 806 (e.g., VT+#V) when the drain current 810 decreases at 811.

As such, Applicants assert that 806 and VT=VT MIN in Figure 8A have overcome the 112 objections. Applicants respectfully request review and approval of Claims 1-20.

Applicants respectfully contend that in Figure 8B, sufficient description is provided for VG=6V, VG=0V, VD=5V, VD=0V, VT=VT MIN, 846, 843 and 831 when programming a second threshold voltage 830. As amended in the paragraph beginning on page 11, line 1, the drain current 835 begins to decrease 836 when the threshold voltage 830 reaches the desired level (e.g., VT=5V) 831 after rising from VT=VT MIN. At that point, the gate voltage drops from VG=6V to VG=0V as shown in Figure 8B at 846. In addition, the drain voltage 840 rises from VD=0V towards VD=5V but drops at 843 when the threshold voltage 830 reaches the desired level (e.g., VT=5V) 831. As such, Applicants assert that VG=6V, VG=0V, VD=5V, VD=0V, VT=VT MIN, 846, 843 and 831 in Figure 8B have overcome the 112 objections. Applicants respectfully request review and approval of Claims 1-20.

Applicants respectfully contend that in Figure 8C, sufficient description is provided for VT=VT MIN when programming a third threshold voltage 860. As amended in the paragraph beginning on page 11, line 12, the threshold voltage 860 is programmed to the level of voltage present on the gate (e.g., 8V) minus the minimum threshold voltage (e.g., VT=VT MIN=1V) which is 7V 861. As such, Applicants

assert that VT=VT MIN in Figure 8C has overcome the 112 objection. Applicants respectfully request review and approval of Claims 1-20.

CONCLUSION

In light of the facts and arguments presented herein, Applicants respectfully request reconsideration of the rejected Claims.

Based on the arguments presented above, Applicants respectfully assert that Claims 1-20 overcome the rejections of record. Therefore, Applicants respectfully solicit allowance of these Claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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Date: 10 MARCH 2005

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